Development of passivating contacts using cost-competitive deposition method for high-efficiency silicon solar cells

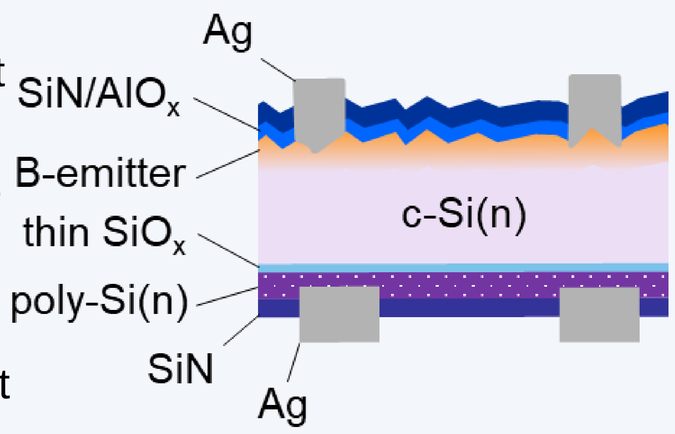
Audrey Morisset[1], Christophe Allebé[2], Antoine Descoeudres[2], Julien Hurni[1], Sofia Libraro[1], Ezgi Genc[1], Franz-Josef Haug[1], Bertrand Paviet-Salomon[2] and Christophe Ballif[1,2]

[1]EPFL, Institute of Electrical and Microengineering (IEM), Photovoltaics and Thin Film Electronics Laboratory (PV-Lab), Maladière 71b, 2002, Neuchâtel, Switzerland
[2]CSEM, Sustainable Energy Center, Rue Jaquet-Droz 1, 2000 Neuchâtel, Switzerland

Context

- TOPCon* is the new mainstream silicon solar cell with conversion efficiencies > 25% in the industry[1]
- LPCVD** is broadly used in the industry to deposit the poly-Si layer that passivates the rear side
- PVD*** is a promising alternative with potential for high throughput and simpler processing
- Within iPrecise and DELAPS projects we aim at integrating PVD poly-Si layers at the rear and front side of high-efficiency silicon solar cells

TOPCon structure



	LPCVD	PVD
Industrial	Yes	Yes
Asymmetric doping	No	Yes
Layer tunability	Low	High
Single side deposition	No	Yes
Production throughput	High	High
Hazardous gases	Yes	Optional
Vacuum	Low	High
Equipment cost	Medium	Medium

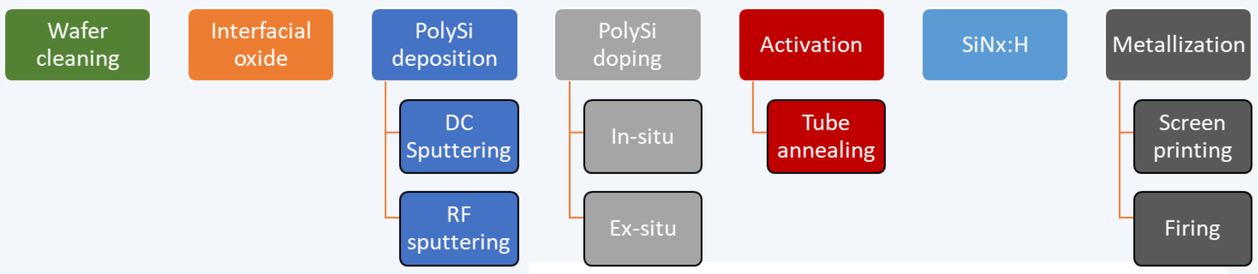
TOPCon: Tunnel Oxide Passivated Contact

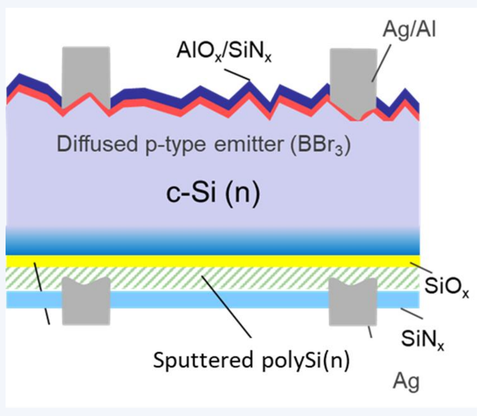
***LPCVD: Low Pressure Chemical Vapour Deposition*
****PVD: Physical Vapour Deposition*

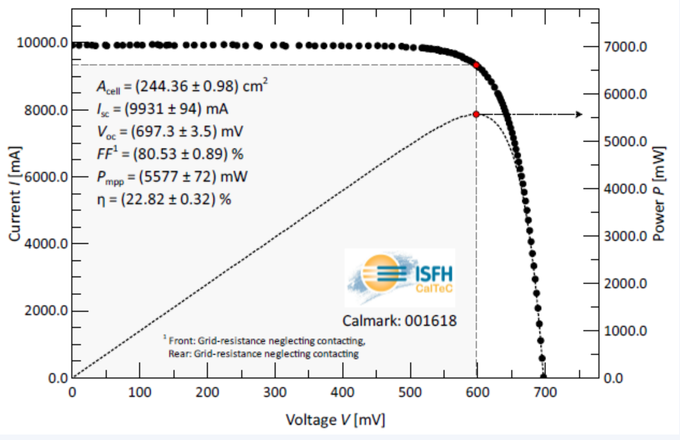
1 – Integration of PVD poly-Si at the rear

- PVD poly-Si layers were optimized to find best compromise between passivation of the silicon substrate and charge carrier collection at the metal electrode
- The optimized layers were integrated at the rear side of TOPCon solar cells featuring a surface area of 244 cm^2. Efficiencies up to 22.8% could be obtained[2]
- Process is currently upscaled to an in-line PVD reactor to demonstrate its potential for industrial manufacturing

Process flow for solar cell fabrication:



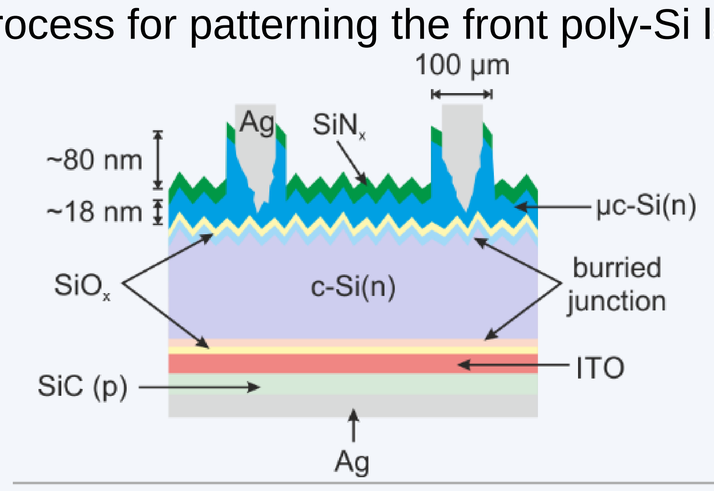




In-line PVD reactor:

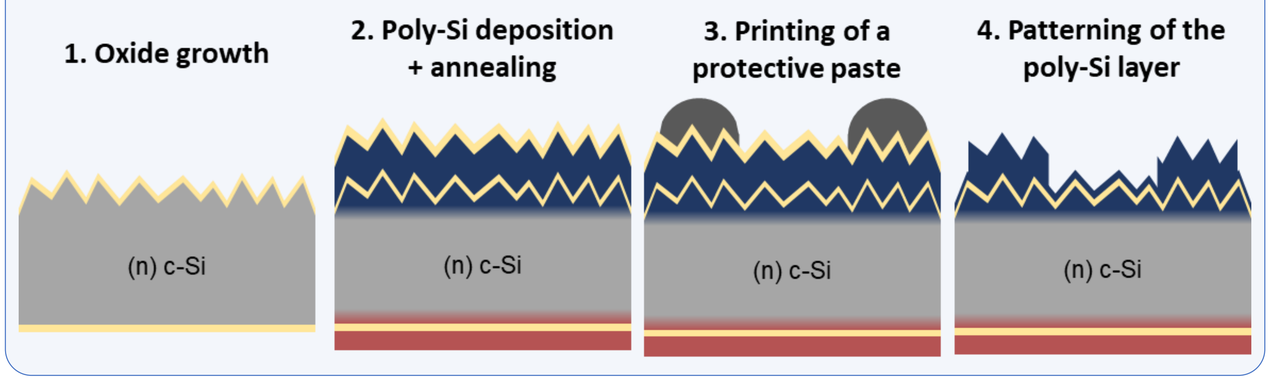
2 – Integration of poly-Si at the front

- To further improve the V_{oc}, a poly-Si passivating layer should also be integrated at the front
- To obtain a high V_{oc} without hindering the photo-generation of charge carriers, the front poly-Si must be patterned so that it remains thick only below the metal contacts
- Proof-of-concept solar cells where fabricated using a mask during deposition of the front poly-Si layer → efficiencies up to 21.7% could be obtained for 2x2 cm^2 devices[3]
- Current work is focused on development of a more industrial-friendly process for patterning the front poly-Si layer



Eff. (%)	FF (%)	V_{OC} (mV)	J_{SC} (mA/cm^2)
21.72	79.7	711.2	38.32

Process considered for industrial patterning of front poly-Si:



Conclusion & Perspectives

- PVD is a promising deposition method to fabricate poly-Si passivating layers with high throughput and simple processing
- The integration of PVD poly-Si layers at the rear side of large area TOPCon devices enabled conversion efficiencies up to 22.8%
- Our current work is focused on upscaling the PVD process and integrating poly-Si layers at the front side of silicon solar cells

References
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